Practice 5. FSK demodulator with PLL

5.1. Objectives

To study the operation of a PLL and its application to demodulate a FSK signal.

5.2. PLL LM565

The LM565 is a general purpose phase locked loop (PLL) containing a stable, highly linear voltage controlled oscillator (VCO) and a double balanced phase detector with good carrier suppression. This device can be used in several kinds of applications: data synchronization, FSK or FM demodulation, coherent demodulation, frequency synthesizers, frequency multiplication, etc.

Both the VCO free-running operation frequency and the filter bandwidth can be adjusted by using external resistors and capacitors. Next, the main features of the device are summarized:

Phase detector
- Input impedance: 5 kΩ
- Output impedance: 3.6 kΩ
- Sensitivity $K_D$: 0.68 V/rad

Voltage controlled oscillator
- Maximum operating frequency: 500 kHz
- Sensitivity $K_O$: $4.1 f_O$ rad/sec·V ($f_O$, VCO freq.)

Locked loop
- Loop gain $K_O K_D$: 2.8 $f_O$ Hz (Supply voltage ±6V)

The VCO free-running frequency is approximately given by:

$$f_0 \approx \frac{0.3}{R_0 C_0}$$  \hspace{1cm} (1)

where $R_0$ and $C_0$ are the external resistor and capacitor which are connected to pins 8 and 9 of the integrated circuit. Therefore, the gain loop is given by:

$$K_0 K_D = \frac{33.6 f_0}{V_C}$$  \hspace{1cm} (2)

being $V_C$ the total supply voltage. The range of frequencies that the loop remains in lock after being initially locked (hold-in range) is
5.3. Practical development

5.3.1. FSK modulator

In figure 1, we show a practical circuit for generating the FSK modulated signal by using a timer NE555. The circuit operation is the following:

a) When the digital modulation signal is at high logic level, the capacitor is charged through the 4.7 kΩ and 22 kΩ resistors, which are connected in parallel to the 10 kΩ resistor. Regarding capacitor discharging, this is performed through the 10 kΩ resistor only. Therefore, the output high-level duration $W_1$ and low-level duration $W_2$ are:

$$W_1 = 0.693(R_0 \parallel R_3)R_2C$$
$$W_2 = 0.693R_2C$$

$$R_1 = 4.7\, \text{kΩ}, R_2 = 10\, \text{kΩ}, R_3 = 22\, \text{kΩ}, C = 47\, \text{nF}$$

b) When the modulation signal is at high logic level, the capacitor charging is carried out through the 4.7 kΩ and 10 kΩ resistors, but a certain amount of the total current through these resistors flows to ground through the 22 kΩ resistor. This complicates the analysis of the circuit but it is clear to understand that the charging will be slower, and then the output high-level duration will be larger than before.

$$W_1 = -\tau \ln \frac{1 - \frac{2}{3}B}{1 - \frac{1}{3}B}$$

$$A = R_1 + R_2 + \frac{R_1 R_2}{R_3}, B = 1 + \frac{R_1}{R_3}, \tau = AC / B$$

As before, the capacitor is discharged through the 10 kΩ resistor only, and then the output low-level duration will be the same.

Therefore, by using this simple circuit we can generate a FSK modulated signal (with digital carrier) whose operation frequencies are about 1 kHz and 1.2 kHz for low and high level, respectively.

1. Implement the next circuit and apply a digital modulation signal with +6V in logic level “1” and 0V in logic level “0”, and frequency about 20 Hz.

2. Observe the modulator output and measure the output frequencies at both logic levels. Compare the obtained experimental results with the theoretical ones given by equations (4) and (5).
5.3.2. FSK demodulator with PLL

In figure 2 is shown the scheme of the FSK demodulation which uses a PLL for recovering the modulation signal.

1. Implement the circuit of figure 2 and disconnect pins 4 and 5 of the PLL (short-circuited with a wire). Observe the free-running frequency of the VCO in pin 4. Modify the potentiometer resistance \( R_0 \) to make this frequency about 1 kHz or slightly superior.

2. Connect pins 4 and 5 again. Observe the phase comparator output (after amplifier) in pins 6 and 7. Compare each of these signals with the demodulated signal in the output pin of the comparator (pin 7 of integrated circuit LM311).
3. Compare the output signals of the VCO with the FSK signal at the PLL input. Finally, compare the retrieved modulation signal (at the comparator output) with the original modulation signal of the signal generator.

5.4. Simulation by using Simulink

Previously to the practical development is recommended to carry out a study about the practical design by using the tool Simulink of the simulation package MatLab.

First of all, implement the PLL shown in figure 3. At its input will be connected a signal generator (sine waveform) whose frequency will be \( f_c = 1 \text{kHz} \). The low-pass filter will be of order 2, and its cut-off frequency will be set to \( f_{\text{cut-off}} = f_c/2 \). The free-running frequency of the VCO will also be \( f_c \), and its sensitivity \( (2f_c/10) \text{Hz/V} \). Add an initial phase shift of 1 rad between the VCO signal and the sine wave from the signal generator. Run a simulation with final time \( 20/f_c \text{s} \) and check how the VCO locks with the input signal with a phase shift of 90° between both of them.

![Figure 3. PLL design](image)

Next, we will observe the PLL recovering of a FSK modulated signal. To do this, implement the FSK modulator and PLL demodulator shown in figure 4. Now, the signal supplied by the generator will be a square waveform with frequency \( f_c/100 \text{Hz} \) (modulation), and the carriers will have frequency values of \( f_1 = 0.9f_c \) and \( f_2 = 1.1f_c \). The switch works as FSK modulator, since the switching is controlled by the digital modulation signal. The sign detector at the PLL output works as comparator being its input signal that used for controlling the VCO frequency oscillation. This signal coincides with a filtered version of the modulation signal. Check as this circuit allows for the demodulation of the FSK signal.
Figure 4. Design of a FSK modulator and demodulator